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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/623,732	07/22/2003	Kyoichi Suguro	04329.2344-02	6071

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FINNEGAN, HENDERSON, FARABOW, GARRETT & DUNNER  
LLP  
901 NEW YORK AVENUE, NW  
WASHINGTON, DC 20001-4413

EXAMINER
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DOAN, THERESA T

ART UNIT	PAPER NUMBER
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2814

MAIL DATE	DELIVERY MODE
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06/11/2007

PAPER

**Please find below and/or attached an Office communication concerning this application or proceeding.**

The time period for reply, if any, is set in the attached communication.

**Office Action Summary**

Application No.

10/623,732

Applicant(s)

SUGURO ET AL.

Examiner

Theresa T. Doan

Art Unit

2814

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --  
Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 03 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

**Status**

- 1) ☒ Responsive to communication(s) filed on 27 March 2007.  
2a) ☒ This action is **FINAL**. 2b) ☐ This action is non-final.  
3) ☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

**Disposition of Claims**

- 4) ☒ Claim(s) 38-41 is/are pending in the application.  
4a) Of the above claim(s) \_\_\_\_\_ is/are withdrawn from consideration.  
5) ☐ Claim(s) \_\_\_\_\_ is/are allowed.  
6) ☒ Claim(s) 38-41 is/are rejected.  
7) ☐ Claim(s) \_\_\_\_\_ is/are objected to.  
8) ☐ Claim(s) \_\_\_\_\_ are subject to restriction and/or election requirement.

**Application Papers**

- 9) ☐ The specification is objected to by the Examiner.  
10) ☐ The drawing(s) filed on \_\_\_\_\_ is/are: a) ☐ accepted or b) ☐ objected to by the Examiner.  
Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).  
Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).  
11) ☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

**Priority under 35 U.S.C. § 119**

- 12) ☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).  
a) ☒ All b) ☐ Some \* c) ☐ None of:  
1. ☐ Certified copies of the priority documents have been received.  
2. ☒ Certified copies of the priority documents have been received in Application No. 09/609,107.  
3. ☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).  
\* See the attached detailed Office action for a list of the certified copies not received.

**Attachment(s)**

- 1) ☐ Notice of References Cited (PTO-892)  
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)  
3) ☐ Information Disclosure Statement(s) (PTO/SB/08)  
Paper No(s)/Mail Date \_\_\_\_\_  
4) ☐ Interview Summary (PTO-413)  
Paper No(s)/Mail Date \_\_\_\_\_  
5) ☐ Notice of Informal Patent Application  
6) ☐ Other: \_\_\_\_\_

### DETAILED ACTION

1. The amendment filed 03/27/07 have being acknowledged and entered. By this amendment, claims 38-39 and newly added claims 40-41 are pending in the application.

#### ***Claim Rejections - 35 USC § 102***

2. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

A person shall be entitled to a patent unless –

(b) the invention was patented or described in a printed publication in this or a foreign country or in public use or on sale in this country, more than one year prior to the date of application for patent in the United States.

3. Claims 38-41 are rejected under 35 U.S.C. 102(b) as being anticipated by Yamazaki (5,306,940) previously cited.

Regarding claim 38, Yamazaki (Fig. 8F) discloses a semiconductor device comprising:

a substrate 101 having a semiconductor layer 103 and a trench (corresponding to the area that occupied by the oxide film 113, 115c, 116a and also see Fig. 8C), the semiconductor layer 103 being an epitaxial layer (column 10, line 49), the trench partitioning the semiconductor layer into a plurality of regions;

an element isolating insulating film (113, 115c, 116a) provided in the trench for partitioning the semiconductor layer 103 into a plurality of element regions, the element isolating insulating film (113, 115c, 116a) having a top surface projecting upward above

Art Unit: 2814

a top surface of the semiconductor layer 103, wherein the element isolation insulating film (113, 115c, 116a) is an oxide film; and

a MOS type element formed within a corresponding one of the element regions and having a gate insulating film 118 and a gate electrode 122a on the gate insulating film 118, wherein:

a difference in height from the substrate between a top surface position of the element isolating insulating film (113, 115c, 116a) and a top surface position of the semiconductor layer 103 is at least three times as large as the thickness of the gate insulating film 118, the top surface position of the element isolating insulating film (113, 115c, 116a) is not higher than a top surface position of the gate electrode 122a, the element isolating insulating film and each of the element regions make an interface which is substantially perpendicular to the top surface of the semiconductor layer 103, the element isolating insulating film (113, 115c, 116a) further having a side surface projecting above the top surface of the semiconductor layer 103 wherein the side surface is substantially perpendicular to the top surface of the semiconductor layer 103, the gate electrode 122a is formed on the gate insulating film 118, the gate insulating film 118 being formed on the top surface of the semiconductor layer 103 in each of the element regions which is not covered with the element isolating insulating film, and the gate electrode 122a is formed on the gate insulating film 118 (Fig. 8F).

Regarding claim 39, Yamazaki (Fig. 8F) discloses a semiconductor device comprising:

Art Unit: 2814

a substrate 101 having a semiconductor layer 103 and a trench (corresponding to the area that occupied by the oxide film 113, 115c, 116a and also see Fig. 8C), the semiconductor layer 103 being an epitaxial layer (column 10, line 49), the trench partitioning the semiconductor layer into a plurality of regions;

an element isolating insulating film (113, 115c, 116a) provided in the trench for partitioning the semiconductor layer 103 into a plurality of element regions, the element isolating insulating film (113, 115c, 116a) having a top surface projecting upward above a top surface of the semiconductor layer 103, wherein the element isolation insulating film (113, 115c, 116a) is an oxide film; and

a MOS type element formed within a corresponding one of the element regions and having a gate insulating film 118, wherein:

a difference in height from the substrate between a top surface position of the element isolating insulating film (113, 115c, 116a) and a top surface position of the semiconductor layer 103 is at least 10nm (column 15, lines 11-12), the top surface position of the element isolating insulating film (113, 115c, 116a) is not higher than a top surface position of a gate electrode 122a, the element isolating insulating film and each of the element regions make an interface which is substantially perpendicular to the top surface of the semiconductor layer 103, the element isolating insulating film (113, 115c, 116a) further having a side surface projecting above the top surface of the semiconductor layer 103 wherein the side surface is substantially perpendicular to the top surface of the semiconductor layer 103, the gate electrode 122a is formed on the gate insulating film 118, the gate insulating film 118 being formed on the top surface of

Art Unit: 2814

the semiconductor layer 103 in each of the element regions which is not covered with the element isolating insulating film, and the gate electrode 122a is formed on the gate insulating film 118 (Fig. 8F).

Regarding claims 40-41, Yamazaki (Fig. 8D) discloses the gate electrode 122a contacts the side surface of the element isolating insulating (113, 115c, 116a) in vertical cross-section perpendicular to a gate length direction of the MOS type element.

### ***Response to Arguments***

Applicant's arguments filed 03/27/07 have been fully considered but they are not persuasive.

4. Applicant argues that "the top surfaces of silicon oxide film 113 and BPSG film 115c of Yamazaki are not above the top surface of N type epitaxial layer 103 of Yamazaki. See Yamazaki, Fig. 8C. In addition, the combination of the silicon oxide film 116a and the LOCOS type field oxide film 110 in Fig. 8C of Yamazaki, which could be argued to correspond to the claimed element isolating insulating film, does not have a side surface that is perpendicular to the top surface of N type epitaxial layer 103".

This argument is not persuasive because Examiner replied on silicon oxide film 113, BPSG film 115c and silicon oxide film 116a of Yamazaki in Fig. 8C for the element isolating insulating film. Therefore, Yamazaki teaches the element isolating insulating film (113, 115c, 116a) having a side surface projecting above the top surface of the

Art Unit: 2814

semiconductor layer 103 wherein the side surface is substantially perpendicular to the top surface of the semiconductor layer 103.

The rest of applicant's arguments have been addressed to the amended claims are considered in the rejections shown above.

### ***Conclusion***

**THIS ACTION IS MADE FINAL.** Applicant is reminded of the extension of time policy as set forth in 37 CFR 1.136(a).

A shortened statutory period for reply to this final action is set to expire THREE MONTHS from the mailing date of this action. In the event a first reply is filed within TWO MONTHS of the mailing date of this final action and the advisory action is not mailed until after the end of the THREE-MONTH shortened statutory period, then the shortened statutory period will expire on the date the advisory action is mailed, and any extension fee pursuant to 37 CFR 1.136(a) will be calculated from the mailing date of the advisory action. In no event, however, will the statutory period for reply expire later than SIX MONTHS from the mailing date of this final action.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Theresa T. Doan whose telephone number is (571) 272-1704. The examiner can normally be reached on Monday, Tuesday and Thursday from 7:00AM - 3:00PM.

Art Unit: 2814

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, WAEL FAHMY can be reached on (571) 272-1705. The fax phone number for the organization where this application or proceeding is assigned is 571-273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see <http://pair-direct.uspto.gov>. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free). If you would like assistance from a USPTO Customer Service Representative or access to the automated information system, call 800-786-9199 (IN USA OR CANADA) or 571-272-1000.

T.D.  
June 4, 2007.



**THERESA DOAN**  
**PRIMARY PATENT EXAMINER**